Desktop Microprocessor Computer Power Systems Using the HIP6018 Controller (HIP6018EVAL1)

Application Note | April 1998 | AN9805

Author: Mike Walters

Introduction

Power systems in desktop microprocessor computers require multiple voltage levels not available from the traditional “silver box” power supply. The HIP6018EVAL1 circuit provides the total power system solution for desktop microprocessor computers when used in conjunction with an ATX power supply. The HIP6018EVAL1 evaluation platform can be configured to meet the various requirements of Intel’s VRM 8.2 and VRM 8.3 guidelines [1]. This document describes the HIP6018EVAL1 reference design, features, and usage guidelines.

Figure 1 shows a simple block diagram of the HIP6018EVAL1 application circuit. The +3.3V, +5V and +12V power inputs are provided by an ATX power supply. The HIP6018 [2] monitors and regulates the three output voltage levels. See the HIP6018 data sheet (File number 4497) for a complete listing of its features and specifications. The HIP6018 controls a synchronous-rectified buck converter to regulate the microprocessor core voltage (VCC_CORE) to a level programmed by a 5-bit digital code. An adjustable linear regulator integrated in the HIP6018 regulates the 2.5V clock voltage (VCC_CLK). An adjustable linear controller drives an external MOSFET to supply the 1.5V GTL bus voltage (VCC_VTT). The linear regulators use the 3.3V from the ATX supply to minimize the power dissipated.

The HIP6018EVAL1 circuit board is designed to show the layout and traces of the power supply portion of a computer motherboard. Included on the board are the ATX input power connector and a Pentium II™, SLOT 1 connector. Motherboard designers should reference the component placement and printed circuit routing of the circuit board. The HIP6018EVAL1 circuit board also contains jumpers and spare component placeholders to facilitate detailed evaluation of the HIP6018.

Quick Start Evaluation

The HIP6018EVAL1 supports testing with standard laboratory equipment or with an ATX power supply and Intel’s EMT test tool. The Slot 1 EMT test tool simulates the transient loading of the Pentium II microprocessor [3]. Figure 2 illustrates the evaluation of the HIP6018 with an ATX supply and an EMT test tool. Simply connect the ATX power supply to the J2 connector and connect the EMT test tool to the Slot 1 connector. Check that the VID jumpers are in place on either the HIP6018EVAL1 board or the EMT tool. Jumpers in both locations may lead to an incorrect core voltage (VCC_CORE) setting. Add other loads to the VCC_VTT and VCC_CLK terminals if desired. Scope probe test points (TP5 and TP6) allow high-bandwidth examination of the output voltages.

Refer to reference [3] for instructions on setting up and using the EMT test tool.

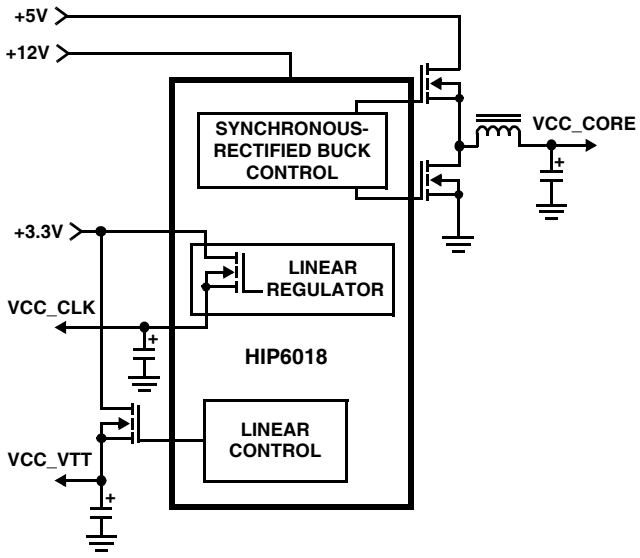


FIGURE 1. HIP6018EVAL1 BLOCK DIAGRAM - THE HIP6018 DERIVES 3 VOLTAGE LEVELS FROM AN ATX SUPPLY

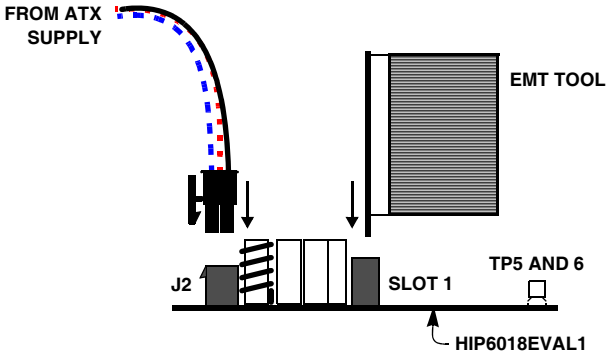


FIGURE 2. EVALUATE THE HIP6018EVAL1 WITH AN ATX POWER SUPPLY AND EMT TEST TOOL

The HIP6018EVAL1 also supports operation with standard laboratory equipment. Table 1 lists the capacity requirement for each of the three power sources and the three loads. Connect a power source to each the $+3.3V_{IN}$, $+5V_{IN}$, and $+12V_{IN}$ terminals and the return for each power source to a GND terminal. Connect individual loads between each output (VCC_CORE, VCC_VTT, and VCC_CLK) and GND. Be sure to set the VID code for the desired VCC_CORE voltage before activating the power sources.

TABLE 1. STANDARD LABORATORY EQUIPMENT REQUIREMENTS

POWER SOURCE		LOAD		
CONNEC-TION	MINIMUM CAPACITY	CONNEC-TION	MAXIMUM CAPACITY	MINIMUM VOLTAGE
$+3.3V_{IN}$	5A	VCC_CORE	20A	1.8V
$+5V_{IN}$	20A	VCC_VTT	4A	1.5V
$+12V_{IN}$	0.1A	VCC_CLK	0.15A	2.5V

HIP6018EVAL1 Reference Design

The HIP6018EVAL1 board features circuits specifically developed for a Pentium II microprocessor computer system with an ATX power supply. Other applications may find these circuits applicable with little modification. The following section describes these circuits in a microprocessor computer system with an ATX power supply.

Output Voltage Droop with Load

The HIP6018EVAL1 uses a droop function to maintain core voltage regulation through load transients. With a high di/dt load transient typical of the Pentium II microprocessor, the largest deviation of the output voltage is at the leading edge of the transient. The droop function prebiases the core voltage high prior to the load transient.

Figure 3 illustrates the static-load droop characteristic. With no-load, the output voltage is above the nominal output level. The output decreases (or droops) as the load increases.

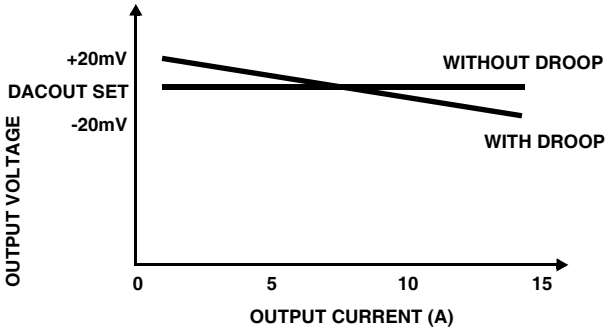


FIGURE 3. THE DROOP CIRCUIT PROGRAMS THE CORE OUTPUT VOLTAGE TO DECREASE WITH INCREASING LOAD

With a dynamic load, the droop function pre-biases the output voltage to minimize the total deviation. Prior to the application of load, the output voltage is biased approximately 20mV above the nominal level (DACOUT set) so that the total deviation allowed at the transient step edge is 20mV more than the transient specification. After the transient edge, core demands the maximum current and the core voltage settles to a level below the DAC setting.

The HIP6004EVAL1 implements the droop function by using the average voltage drop across the output inductor. The average voltage drop equals the DC output current multiplied by the DC winding resistance of the output inductor. An averaging filter (consisting of R4 and C40 in the schematic) reconstructs the voltage across the winding resistance. This filter communicates both the output voltage and droop information back to the PWM controller. The resistor (R9) sets the light-load core voltage above the DAC program level.

ATX Power Control

The HIP6018EVAL1 provides an ATX power control interface circuit as shown in Figure 4. The circuit enables the main outputs of the ATX supply and latches off the ATX supply when the HIP6018 detects a fault. Users may choose to implement this function into other power monitoring and control circuits found on the motherboard.

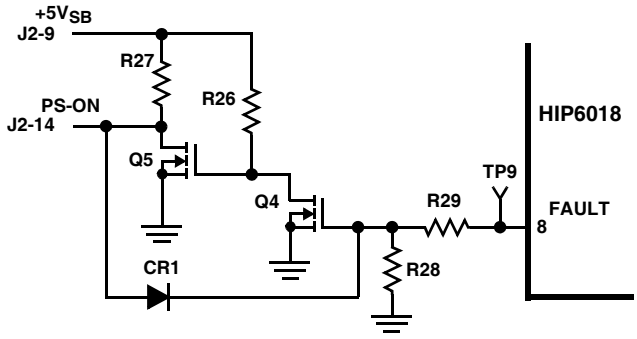


FIGURE 4. ATX POWER CONTROL CIRCUIT LATCHES ATX SUPPLY OFF AFTER FAULT

A +5V standby source ($+5V_{SB}$ - pin 9 on connector J2) is available when the ATX supply is “on”. The remaining ATX outputs are controlled by the PS-ON signal (pin 14 on connector J2). Holding PS-ON to a TTL low level enables the main outputs of the ATX supply. Transistor, Q5 initially turns-on to enable the ATX supply as the +5V standby source builds up to its steady-state level. The transistor, Q4 turns-on in the event of a fault (HIP6018, pin 9 - FAULT = high) to disable the main outputs of the ATX power supply. The diode, CR1 maintains Q4 on as the +12V source on VCC decays (FAULT also decays) and keeps the ATX supply latched off. The circuit is reset by cycling the ATX power supply off then on.

Printed Circuit Board

The HIP6018EVAL1 uses a 4-layer printed circuit board with 2 ounce copper (see Figure 9-13). The component layout and circuit routing is designed to show the power portion of a typical computer motherboard. Included on the board are the ATX input power connector and a Pentium II, SLOT 1 connector. Note that the component side of the board (Figure 10) contains a serpentine trace to the drain of external linear MOSFET, Q4. This trace is recommended, but not necessary for circuit operation. The serpentine trace provides resistance that off loads some of the power dissipation from the external linear MOSFET, Q4. Motherboard designers should reference the

component placement and printed circuit routing of the circuit board. Of course, the test points and spare component footprints of the HIP6018EVAL1 board can be eliminated from the final motherboard.

HIP6018 Performance

Efficiency

Figure 5 shows the laboratory-measured efficiency of the HIP6018EVAL1 versus core load current, for a +5V input and with 100 linear feet per minute (LFM) of airflow. The efficiency is shown for VID settings (DACOUT) of 2.0V and 2.8V. The linear regulator output (VCC_CLK and VCC_VTT) are not loaded.

Core Voltage Transient Response

Figure 6 shows the core output transient response for a 0.5A to 14.4A step load change. The transient load is provided by Intel's EMT (Electrical, Mechanical, Thermal) test tool [3]. The core voltage setting is 2.0V and the transient slew rate is 30A/μs. Also shown in Figure 6 is the transient limits for a 2.0V setting according to the VRM 8.2 guidelines [1]. Note the output voltage at full load is lower than the voltage at light-load. This static characteristic is shown in Figure 3.

Core Over-Voltage Protection

Figure 7 shows the response of the HIP6018EVAL1 circuit to the worst-case over-voltage condition. The drain of the upper MOSFET is shorted to its source with an short external wire and the HIP6018EVAL1 is powered on with an ATX power supply. Under this condition, the core voltage (VCC_CORE) responds as shown in Figure 7.

Figure 7A shows the response of the over-voltage protection with the ATX power control circuit (shown in Figure 4) enabled. Initially, the core voltage (VCC_CORE) follows the $+5V_{IN}$ until it reaches 1.26V. The $+5V_{IN}$ continues to increase, but the lower MOSFET is modulated on and off to regulate the core voltage to 1.26V. This operation continues until the $+12V_{IN}$ supply reaches the POR threshold at approximately 16ms. At this point, the VID inputs set the over-voltage trip level to 115% of the DACOUT level. The DACOUT setting for Figure 7 is 2.8V and the over-voltage trip level is 3.22V. The core voltage increases to this level and over-voltage comparator trips. This set the FAULT pin high and turns-on the lower MOSFET. The core voltage is held to 3.22V and the ATX supply is commanded off by the ATX power control circuit. This causes the core and supply voltages to decrease.

Figure 7B shows the response of the over-voltage protection without the ATX power control circuit. In this case, the fuse, F1 opens to disconnect the input supply. Before the power-on reset (POR), the HIP6018 limits the core voltage to 1.26V in the same manor described above. After the $+12V_{IN}$ supply reaches the POR threshold, the VID inputs set the DACOUT level and the over-voltage trip level. The lower MOSFET is modulated on and off to regulate the core voltage to the over-voltage level (115% of DACOUT) and the FAULT pin goes high. The input current increases until the fuse, F1 opens at 40ms. This causes the core and $+5V_{IN}$ voltages to decrease. The FAULT pin continues high until the $+12V_{IN}$ power is removed. Note that the maximum processor core voltage is limited to 3.22V (= 2.8V x 1.15).

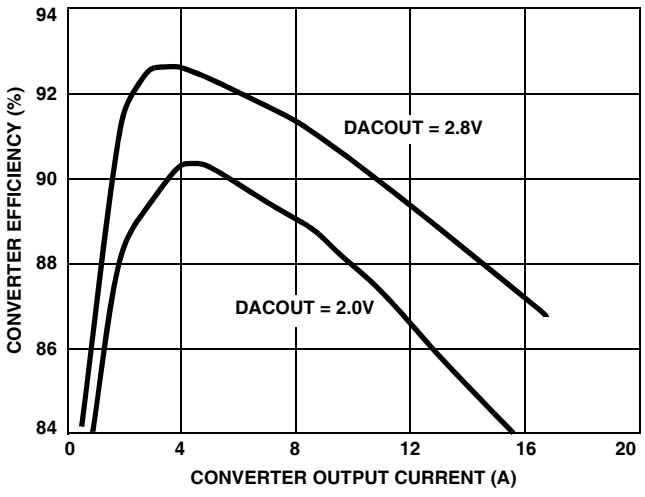


FIGURE 5. HIP6018EVAL1 MEASURED EFFICIENCY

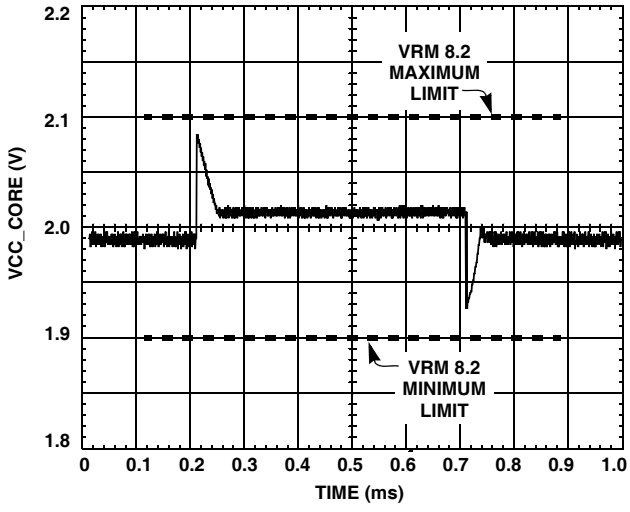


FIGURE 6. CORE OUTPUT VOLTAGE RESPONSE TO 14.4A TRANSIENT WITH INTEL's EMT TOOL: DACOUT SETTING = 2.0V

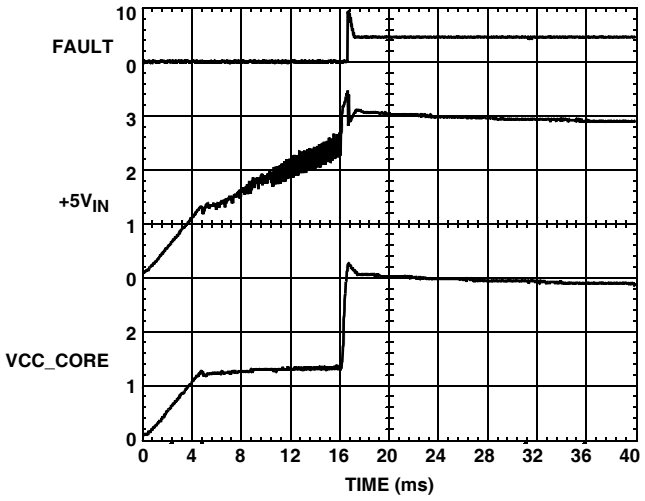


FIGURE 7A. HIP6018EVAL1 OVER-VOLTAGE PROTECTION WITH ATX POWER CONTROL CIRCUIT - APPLYING POWER WITH SHORTED UPPER MOSFET MAINTAINS VCC_CORE AT SAFE LEVELS AND CAUSES THE ATX SUPPLY TO SHUTDOWN

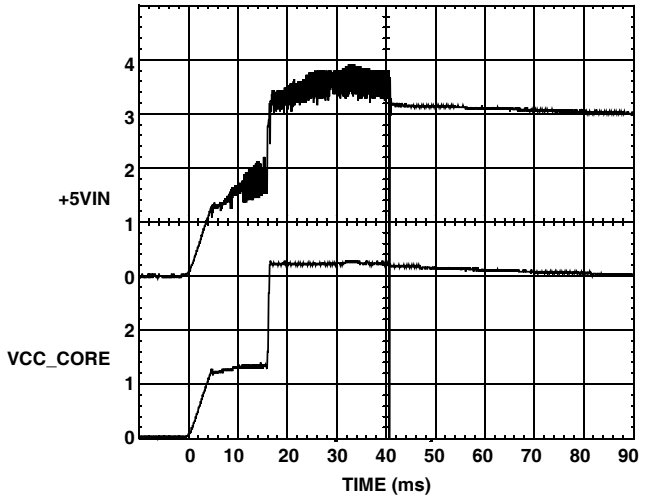


FIGURE 7B. HIP6018EVAL1 OVER-VOLTAGE PROTECTION WITHOUT ATX POWER CONTROL CIRCUIT - APPLYING POWER WITH SHORTED UPPER MOSFET MAINTAINS VCC_CORE AT SAFE LEVELS AND BLOWS THE INPUT FUSE, F1 TO INTERRUPT POWER

HIP6018EVAL1 Modifications

The HIP6018EVAL1 board accommodates additional input and core output capacitance. As supplied the HIP6018EVAL1 meets the requirements of Intel's VRM8.1 guideline. When fully populated, the HIP6018EVAL1 is conservatively designed to meet all the requirements of Intel's VRM 8.2 guideline under worst-case conditions. This design philosophy limits the maximum junction temperature to 115^{o}C with an ambient temperature of 50^{o}C at the maximum loading. Additionally, we use the capacitor vendor's maximum impedance value to select the type and number of output capacitors needed to meet the sever load transient of the guidelines. Users should feel free to modify the design based upon their understanding of the component characteristics and system loading.

Core Output Capacitance

The number of output capacitors and their type is determined by the capacitor's maximum equivalent series resistance (ESR) at high frequency (usually 100kHz) rather than the capacitance value. The ESR determines the output ripple voltage and output voltage transient response. For microprocessor loads, the transient current step ultimately determines the number of capacitors necessary for a given output regulation limit.

Intel specifies the maximum current demand on the microprocessor core based upon executable code know to draw large power. This code toggles the maximum number of processor transistors and can be used to test the power system. Toggling the processor's STPCLK pin while running this code provides a load current transient on the power system. In practice, the actual maximum current and peak load transient has been observed to be less than the value specified by Intel. Users should determine the maximum core transient current step in order to determine the number of capacitors necessary.

As supplied, the HIP6018EVAL1 meets the transient voltage limits of Intel's VRM 8.1. This guidelines specifies a worst case transient of 14.2A at 2.8V. Figure 8 shows the recommended number of output capacitors necessary for the core output to meet the flexible motherboard requirements of VRM8.2 as function of the transient load step. The worst case for this quideline is for 2.0V. The number of capacitors was determined from the following equation which relates the ESR and ESL of the capacitor to the transient load step (ΔI) and the voltage limit (ΔVo):

$$\text{NumberCaps} = \frac{\text{ESL} \bullet (di/dt) + \text{ESR} \bullet \Delta I}{\Delta Vo}$$

The ESR of the capacitor dominates the transient voltage response to a step in current. The maximum ESR of core output capacitors used on the evaluation board, as specified at 100kHz, is 69mΩ per part. The total ESR on the core output (ESR_{CORE}) is the parallel combination of all the capacitors on the core output. ESR_{CORE} is determined by dividing the specified maximum ESR of a capacitor by the total number of capacitors (NumberCaps in equation above). Using the HIP6018EVAL1's 7 core output capacitors as an example, the ESR_{CORE} is 9.9mΩ maximum. Other capacitors can be used to meet the guidelines if the parallel combination of all the core output capacitors is equivalent to the ESR_{CORE}.

Input Capacitor

The input capacitors on the HIP6018EVAL1 (C1 - C7) supply the RMS current of the PWM converter. The maximum RMS current (at full load) determines the number of input capacitors

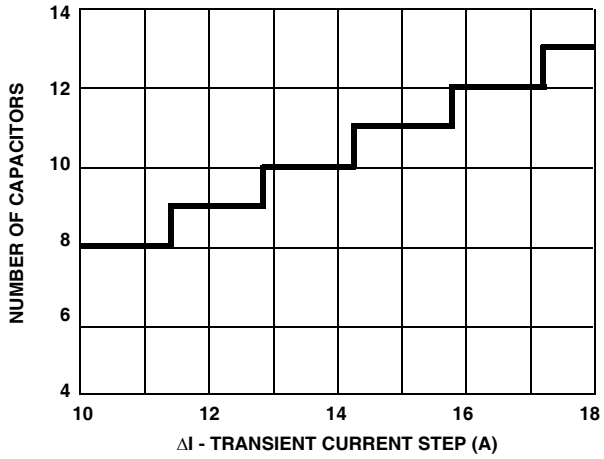


FIGURE 8. GIVEN THE MICROPROCESSOR TRANSIENT CURRENT STEP USE THE APPROPRIATE NUMBER OF CAPACITORS TO MEET THE FLEXABLE MOTHERBOARD REQUIREMENTS OF VRM8.2

as limited by their RMS rating. The maximum RMS current is approximately one half of the load current. The input capacitors on HIP6018EVAL1 each have a ripple current rating of 750mA at 105^{O}C. The 7 capacitors are capable of supporting a 10.5A load. The voltage rating at maximum ambient temperature of the input capacitors should be at least 1.25 to 1.5 times the maximum input voltage.

Overcurrent Protection

The switching regulator utilizes a low loss current-sensing technique to detect an overcurrent event. The voltage drop across the upper MOSFET $r_{DS(ON)}$ is compared with a user-adjustable reference voltage generated by an internal current source across an external resistor. When the voltage across the MOSFET exceeds the preset threshold, the controller shuts down and initiates a soft-start cycle. If the condition persists after three consecutive overcurrent events, the controller latches off. Removing the over load and cycling the bias voltage (+12Vin) restores the circuit to its operating mode. The R_{OCSET} resistor value is set to trip above the maximum expected load current. Its value is dependent upon a number of factors including the MOSFET's maximum $r_{DS(ON)}$, junction temperature, and output inductor ripple current.

Table 2 shows the recommended MOSFET and OCSET resisters for various output current levels. This table assumes a junction temperature of 150°C, a gate driven to 12V with an input of 5V and a output inductor ripple current of ±1A. The maximum anticipated core current should be below the I_{CORE} value shown in Table 2.

TABLE 2. OCSET RESISTOR SELECTION

I_{CORE} A MAX	MOSFET		R_{OCSET}, R2 Ω
	PART NUMBER	$r_{DS(ON)}$ MAX	
16.9	HUF76143	5.5mΩ	1K
20.2	HUF76143	5.5mΩ	1.2K
12.4	HUF76139	7.5mΩ	1K
14.8	HUF76139	7.5mΩ	1.2K
17.3	HUF76139	7.5mΩ	1.4K
10.3	HUF76137	9mΩ	1K
12.4	HUF76137	9mΩ	1.2K
14.4	HUF76137	9mΩ	1.4K

MOSFET Selection

The HIP6018EVAL1 board can accommodate multiple MOSFET package styles. Each placeholder can accommodate TO-263, TO-252 and TO-220 package connections. The output loading and the thermal environment ultimately dictate the MOSFET selected. For the core output, the upper MOSFET (Q1) should be selected according to Table 2 above. The lower MOSFET (Q2) should be selected for $r_{DS(ON)}$ to minimize the power dissipation.

Output Voltages

The core output voltage is adjusted by the VID jumper combination. Please refer to the HIP6019 data sheet for a comprehensive table detailing the VID combinations and the resultant output voltages. The no-load core voltage is adjusted above the DACOUT level according to the following equation:

$$V_{VCC-CORE} = V_{DACOUT} \bullet \left(1 + \frac{R4 + R8}{R9}\right)$$

The output voltage of the linear regulator and controller is set by a resister divider and a bandgap voltage reference, V_{REF}. These outputs can be set as low as 1.26V or as high as the 3.3V input voltage. The steady-state DC output voltages is: for the linear controller and

$$V_{VCC-VTT} = V_{REF} \bullet \left(1 + \frac{R11}{R12}\right)$$

$$V_{VCC-CLK} = V_{REF} \bullet \left(1 + \frac{R13}{R14}\right)$$

for the linear regulator.

V_{REF} = HIP6019 reference voltage (typically 1.267V)

Conclusion

The HIP6018EVAL1 board lends itself to a wide variety of high-power DC-DC microprocessor converter designs. The flexibility allows the designer to quickly modify for applications with various requirements. The printed circuit board accommodates all the necessary components for operation up to 19A.

References

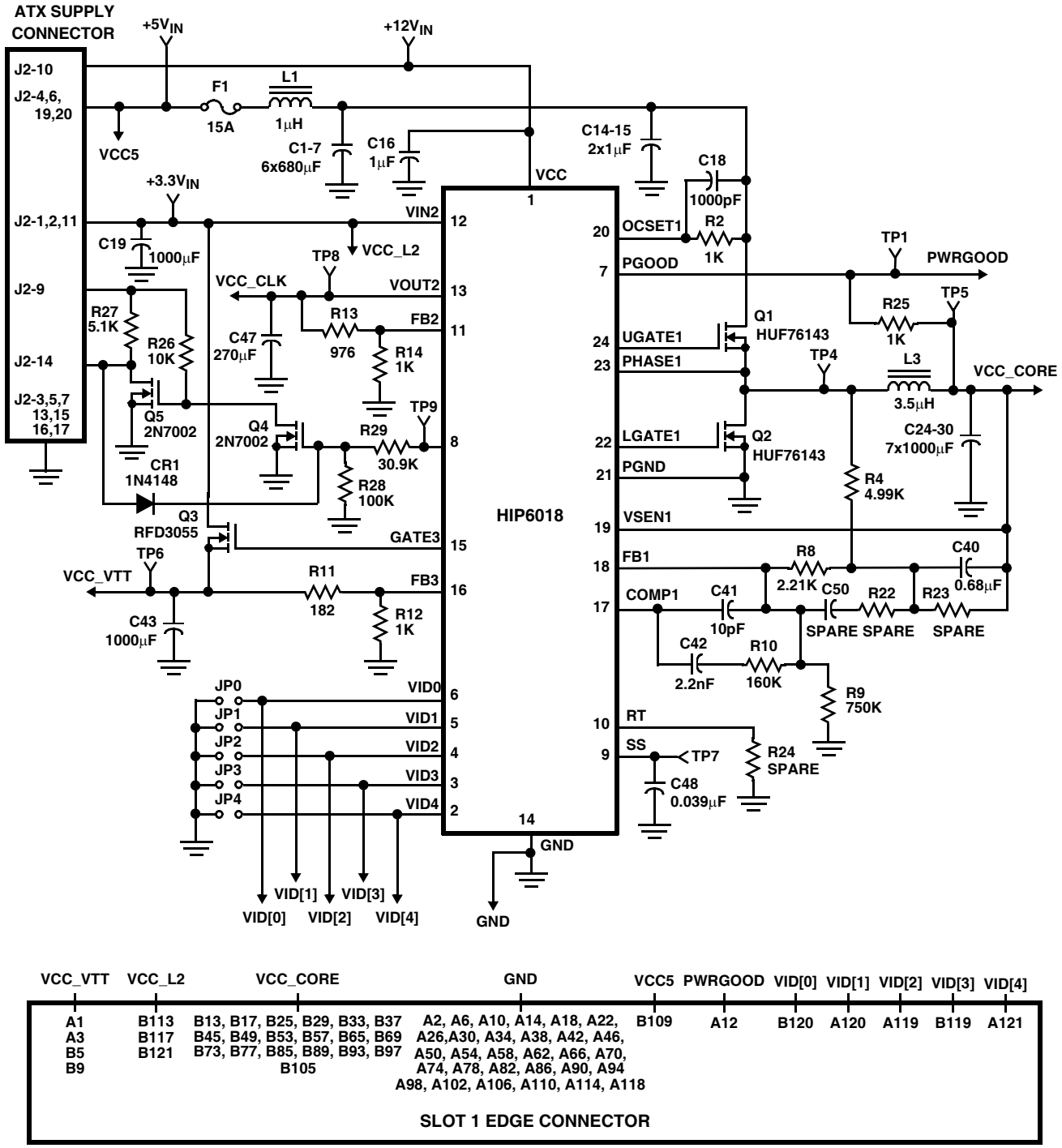
For Intersil documents available on the internet, see web site http://www.intersil.com.

[1] VRM8.2 DC-DC Converter Design Guidelines Rev 1.0, Intel Corporation.

[2] *HIP6018 Data Sheet*, Intersil Corporation, FN4497.

[3] Slot 1 Test Kit, Intel # EUCDSLOTKIT1.

HIP6018EVAL1 Schematic



Bill of Materials for HIP6018EVAL1

REF	PART NUMBER	DESCRIPTION	PACKAGE	QTY	VENDOR
C1-7	10MV680GXL	Aluminum Capacitor, 10V, 680µF	Radial 8x20	7	Sanyo
C8-11, C44-46	spare	Aluminum Capacitor	Radial 8x20	3	
C14-16	1206YZ105MAT1A	Ceramic Capacitor, X7S, 16V, 1.0µF	1206	3	AVX
C18	1000pF Ceramic	Ceramic Capacitor, X7R, 25V	0805	1	Various
C19, C24-30, C43	6MV1000GX	Aluminum Capacitor, 6.3V, 1000µF	Radial 8x20	9	Sanyo
C31-36	spare	Aluminum Capacitor	Radial 8x20	6	
C40	0.68µF Ceramic	Ceramic Capacitor, X7R, 16V	0805	1	AVX / Panasonic
C41	10pF Ceramic	Ceramic Capacitor	0805	1	Various
C42	2.2nF Ceramic	Ceramic Capacitor	0805	1	Various
C47	6MV270GX	Aluminum Capacitor, 6.3V, 270µF	Radial 6.3x11	1	Sanyo
C48	0.039µF Ceramic	Ceramic Capacitor, X7R, 16V	0805	1	Various
C50	spare	Ceramic Capacitor	0805		
CR1	DL4148	General Purpose Diode	DL-35	1	Various
F1	251015A	Miniature Fuse, 15A	Axial	1	Littelfuse
L1	PO720	1µH Inductor, 7T of 16AWG on T50-52 core	Wound Toroid 18x18x9	1	Pulse
L3	PO716	3.5µH Inductor, 9T of 16AWG on T60-52 core	Wound Toroid 20x20x10	1	Pulse
Q1, Q2	HUF76139S3S	UltraFET™ MOSFET, 30V, 7.5mΩ	TO-263	2	Intersil
Q3	RFD3055SM	UltraFET MOSFET, 60V, 150mΩ	TO-252	1	Intersil
Q4, Q5	2N7002TR-ND	MOSFET, 60V, 7.5Ω	SOT-23	2	Zetex
R2, R12, R14, R25	1kΩ	Resistor, 1%, 0.1W	0805	4	Various
R4	4.99kΩ	Resistor, 1%, 0.1W	0805	1	Various
R8	2.21kΩ	Resistor, 1%, 0.1W	0805	1	Various
R9	750kΩ	Resistor, 1%, 0.1W	0805	1	Various
R10	160kΩ	Resistor, 5%, 0.1W	0805	1	Various
R11	182Ω	Resistor, 1%, 0.1W	0805	1	Various
R13	976Ω	Resistor, 1%, 0.1W	0805	1	Various
R26	10kΩ	Resistor, 5%, 0.1W	0805	3	Various
R27	5.11kΩ	Resistor, 1%, 0.1W	0805	3	Various
R28	100kΩ	Resistor, 1%, 0.1W	0805	1	Various
R29	30.9kΩ	Resistor, 1%, 0.1W	0805	1	Various
R22-24	spare		0805		
	71796-0001 145251-1	Slot 1 Edge Connector		1	Molex AMP
J2	39-29-9203	ATX Supply Connector		1	Molex
+3.3V_{IN}, +5V_{IN}, +12V_{IN}, GND, VCC_CORE, VCC_CLK, VCC_L2	1514-2	Terminal Post		12	Keystone
TP5, TP6	1314353-00	Test Point, Scope Probe		2	Tektronics
TP1, TP4, TP7-9	SPCJ-123-01	Test Point		6	Jolo
JP0-4	68000-236 71363-102	Header Jumper		4	Burg
U1	HIP6018	PWM and Dual Linear Controller	SOIC-24	1	Intersil

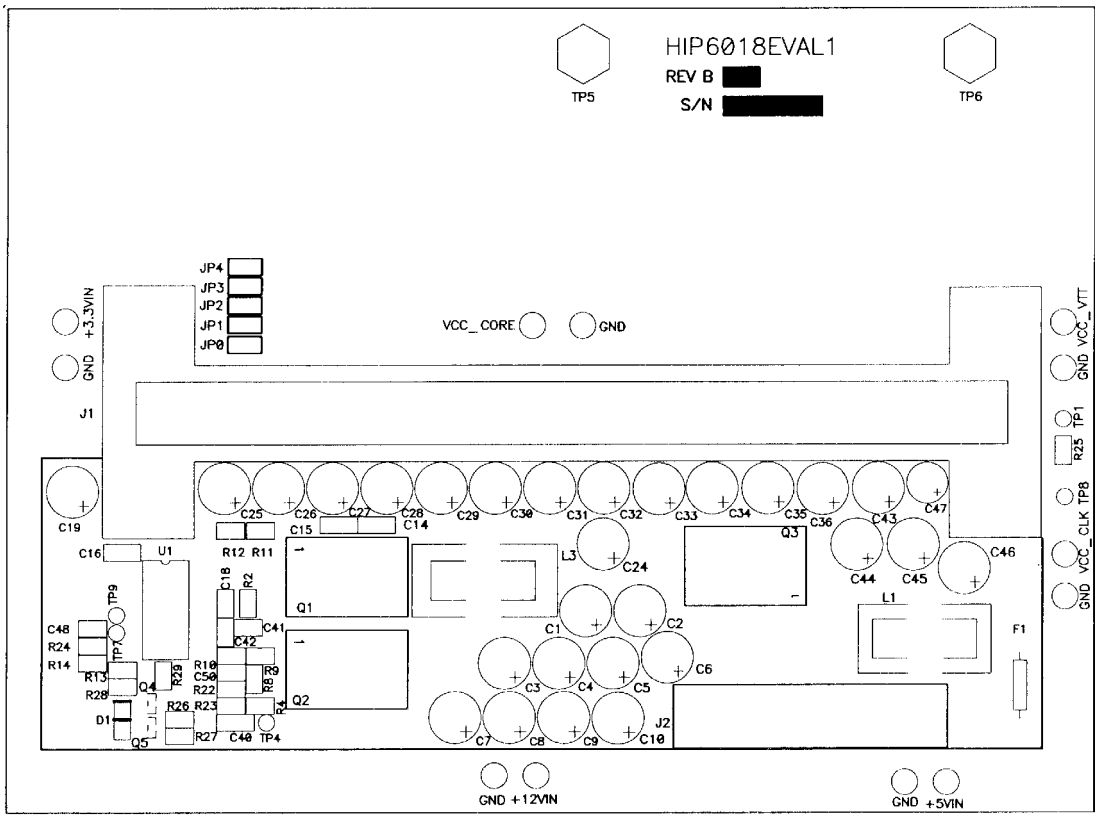


FIGURE 9. HIP6018EVAL1 COMPONENT LAYOUT

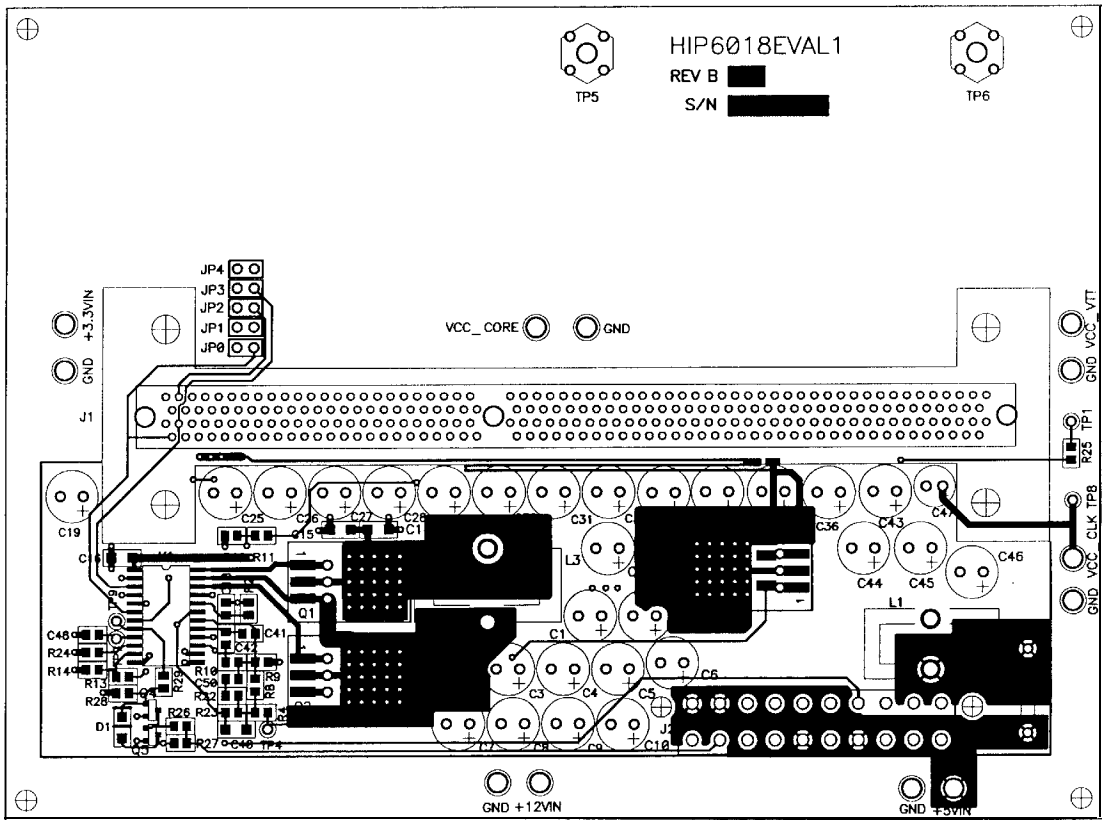


FIGURE 10. HIP6018EVAL1 TOP CIRCUIT LAYER (COMPONENT SIDE)

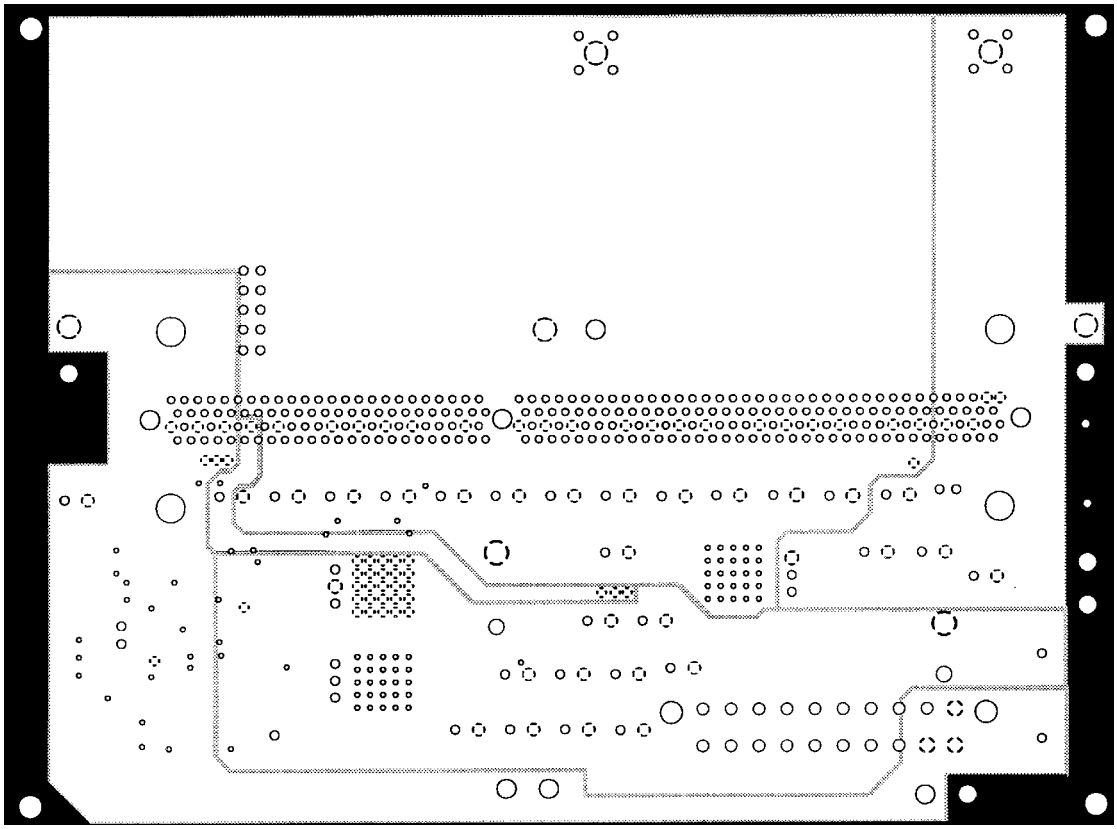


FIGURE 11. HIP6018EVAL1 POWER ISLAND CIRCUIT LAYER

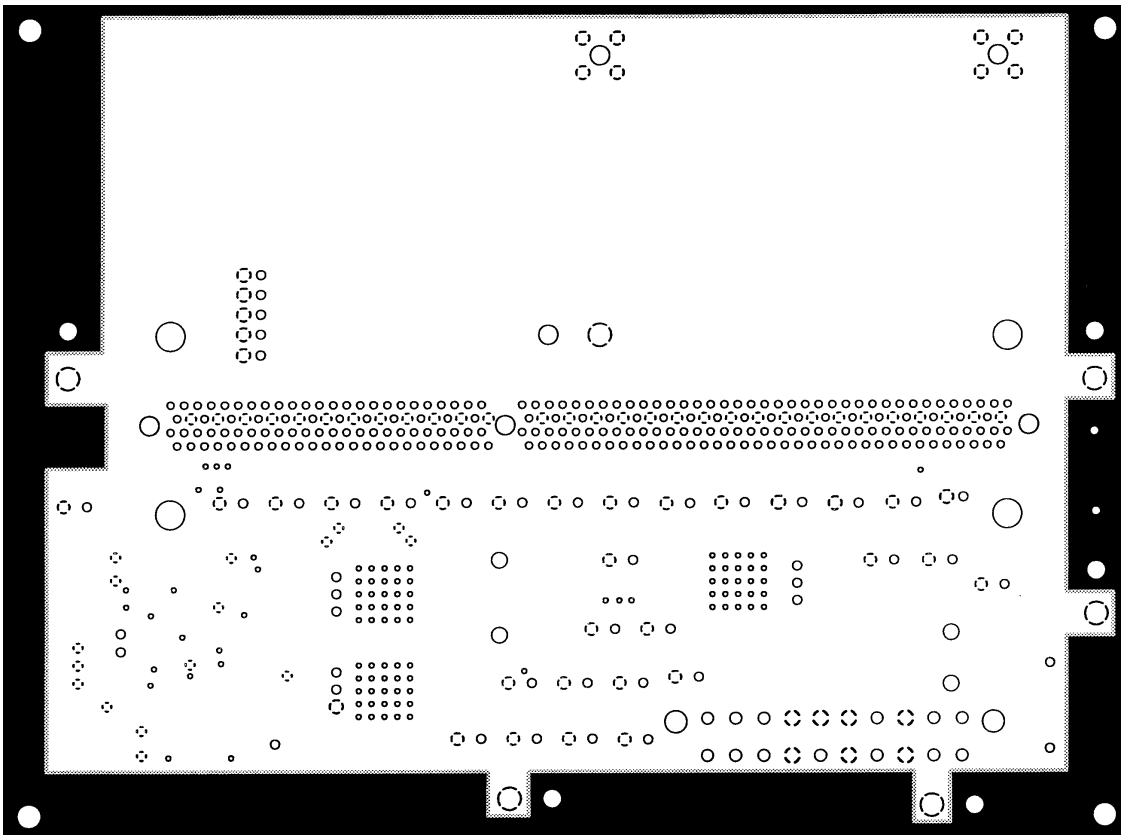


FIGURE 12. HIP6018EVAL1 GROUND LAYER

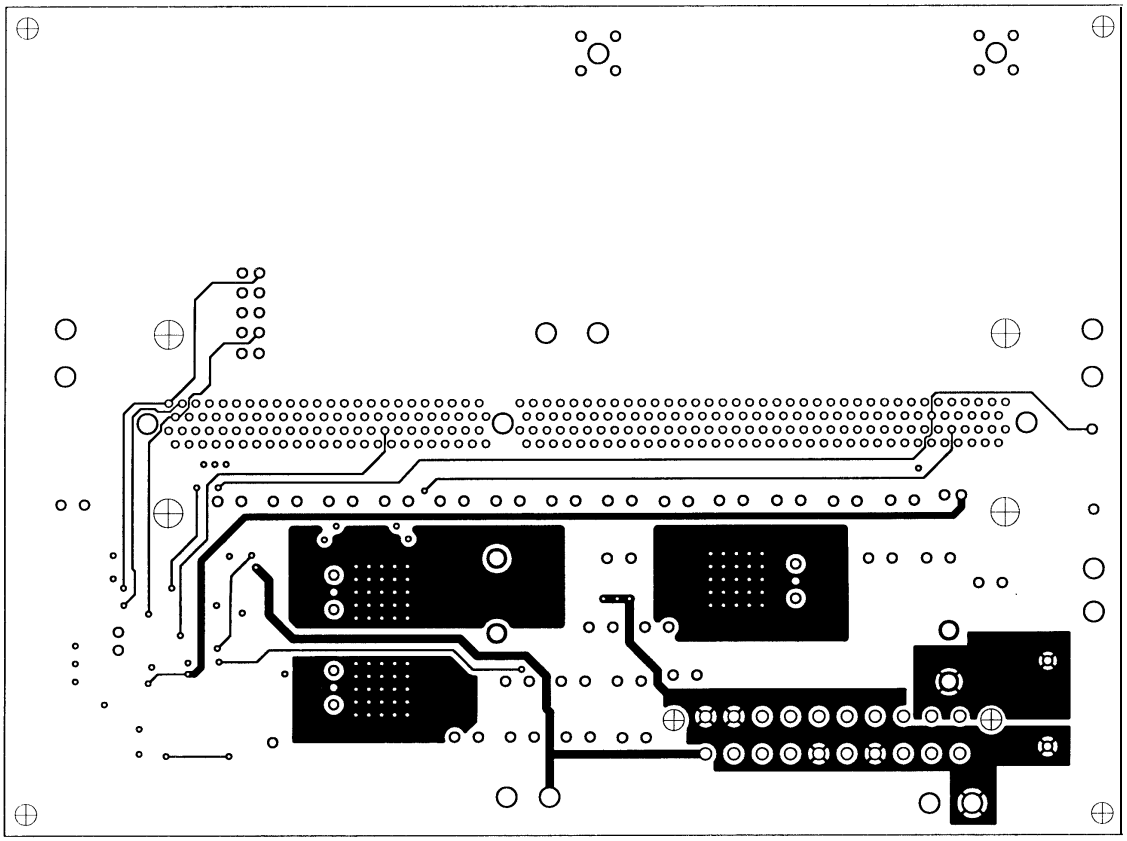


FIGURE 13. HIP6018 BOTTOM CIRCUIT LAYER (SOLDER SIDE)